REMARKS/ARGUMENTS

The rejection of claims 1 - 10, and 12-18 under 35 U.S.C. 102(e) as being anticipated by the patent to Kimura et al. (US 6,806,428 B1), and the rejection of claim 11 under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. in view of Okabe et al. (US 6,757,178 B2), both respectfully traversed.

Regarding the rejection of independent claim 1, the disclosure of Kimura et al. suggests the use of a chip component made to the exact size of corresponding holes to be deposed therein, to function as a passive component; however, contrary to Kimura et al., the present invention use passive component materials (materials of a resistor or a capacitor etc) to fill into openings so as to form the passive component (at least supported by the preferred embodiments of the specification). In addition, the present invention also suggests that the electrically conductive layers formed over the upper and lower surfaces of the core layer fully cover the core layer and the upper and lower surfaces of the passive component material. Thereby forming such a distinctive structure to allow the passive component materials of the present invention to 'be fitted into any opening of any size quickly and easily in a simple manufacturing process without worrying about the potential component matching problems between the chips component and the holes in Kimura et al. (which requires extra effort and cost to avoid such occurrences).

In addition, the present invention further suggests several readily alternative ways, by alternating the size of the openings, by adapting to either the serial or parallel electrical interconnection between the passive component materials or by changing the materials of the passive component materials, to form desired capacitance or resistance. However, penetration holes disclosed in Kimura et al. are only employed for the insertion of the chip components. Seemingly, Kimura et al employs dissimilar ways to determine the capacitance or the resistance thereof, whereas none of the suggested ways is equivalent to the disclosure of present invention.

Furthermore, the structure disclosed in Kimura et al, having circuit wirings formed over the upper and lower surface of the resin substrate, penetration holes

formed for inserting chip components and the connection electrodes formed on the chip components and resin substrate before conductive resin formed thereon to electrically couple the chip components to the circuit wiring, is different from the structure of the present invention; unlike Kimura et al., the structure of the present invention has the passive components (namely, passive component materials) embedded in the openings of the core layer with a complete coverage of the conductive layer over the surfaces of core layer and the passive components directly.

Regarding the rejection of independent claim 12, by comparing the manufacturing process suggested by Kimura et al. (figures 6(a) to 6 (i); column 4 and column 5) to the manufacturing process of the present invention several distinguishable procedures are clearly indicated. For instance, in Kimura et al, formation of the wiring patterns on both sides of resin substrate happened first, and following by the formation the penetration holes (for inserting the chip components), the insertion of the chip components into the penetration holes and additional formation of connection electrodes so as to allow chip components to electrically interconnect to the circuit wirings. On the contrary, the manufacturing process of the present invention is proceeded in a different order like filling the openings formed on the core layer with the passive component materials, fully covering the upper and lower surfaces of the core layer and the passive components by the conductive layer, patterning the conductive layer to form conductive traces and then electrically interconnecting the patterned conductive traces to the passive components, so as to form the electrical interconnections of the passive components.

More particularly, in Kimura et al, the procedure of deposing the chip components, and the procedure of electrically interconnecting the chip components and the conductive traces are proceeded separately and individually through various stages; however, the present invention is capable of forming the circuit wirings and electrically interconnecting the passive components simultaneously. Therefore the present invention not only comprises several novel and inventive steps of manufacturing process which are arranged in a different order from Kimura et al., but also simplifies the manufacturing process and reduces the cost of production. Furthermore, forming the conductive traces directly from the patterned conductive

layer over the surfaces of the core layer for electrically interconnecting the passive components serially or parallel facilitates the modularization of the passive components, whereby another outstanding inventive characteristic of the present invention being proved against the referenced documents once again.

Accordingly, the structure or the method thereof in the present invention are not only novel, distinguishable and inventive, but also sustain advantage over referenced documents.

In view of the foregoing discussion, independent claims 1 and 12 are believed to be patentable. Inasmuch as independent claims 1 and 12 are believed to be patentable, the remaining claims in this patent application, which depend therefrom, are likewise believed to be patentable. Accordingly, a Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge payment of any fees required associated with this communication or credit any overpayment to Deposit Account No. 50-0337. If an extension of time is required, please consider this a petition therefor and charge any additional fees which may be required to Deposit Account No. 50-0337. A duplicate copy of this paper is enclosed.

Respectfully submitted,

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Amendments to the Drawing:

The attached sheet of drawings includes a change to Figs. 3A. This sheet replaces the original sheet. In Figure 3A, a sectional line has been added showing that Figure 3B is a sectional view on Figure 3A.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

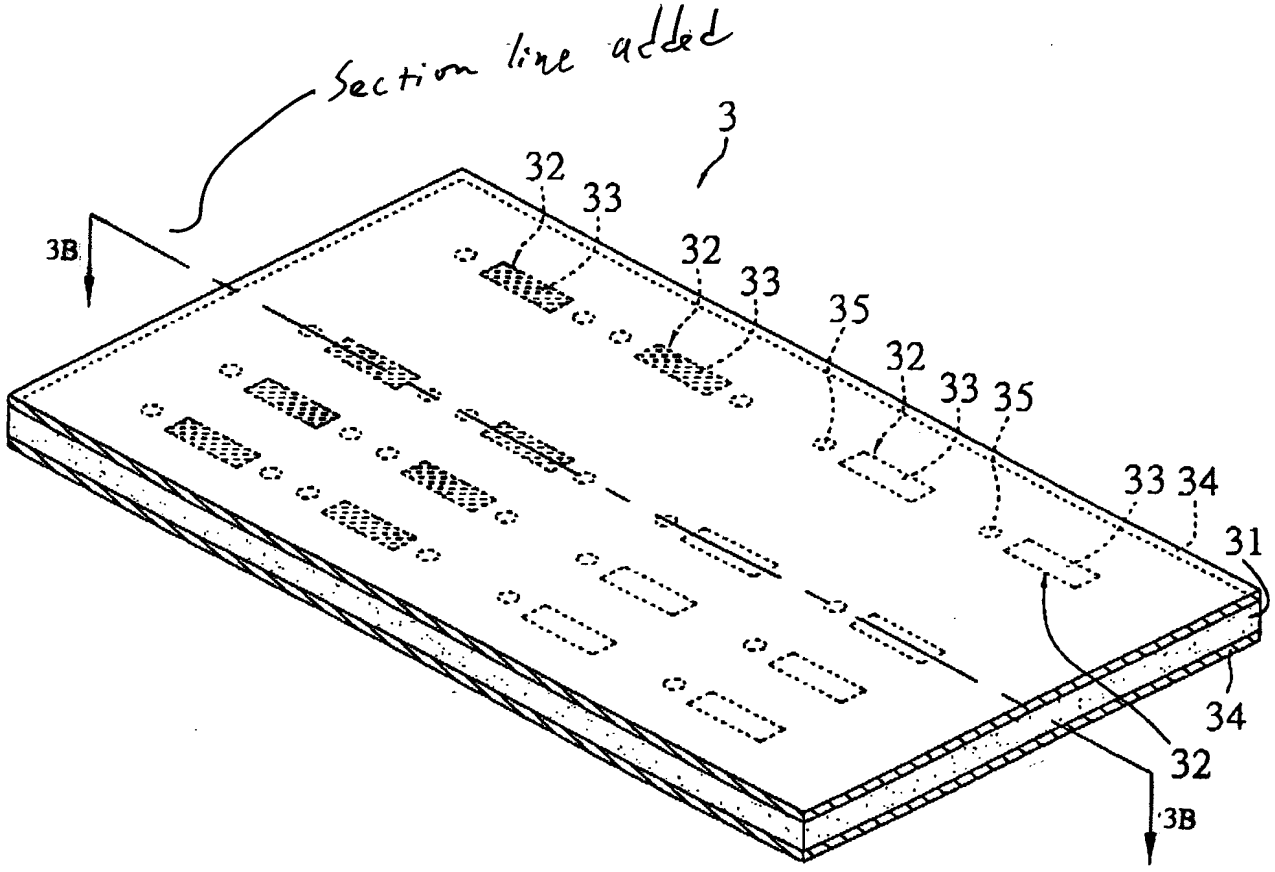

FIG. 3A

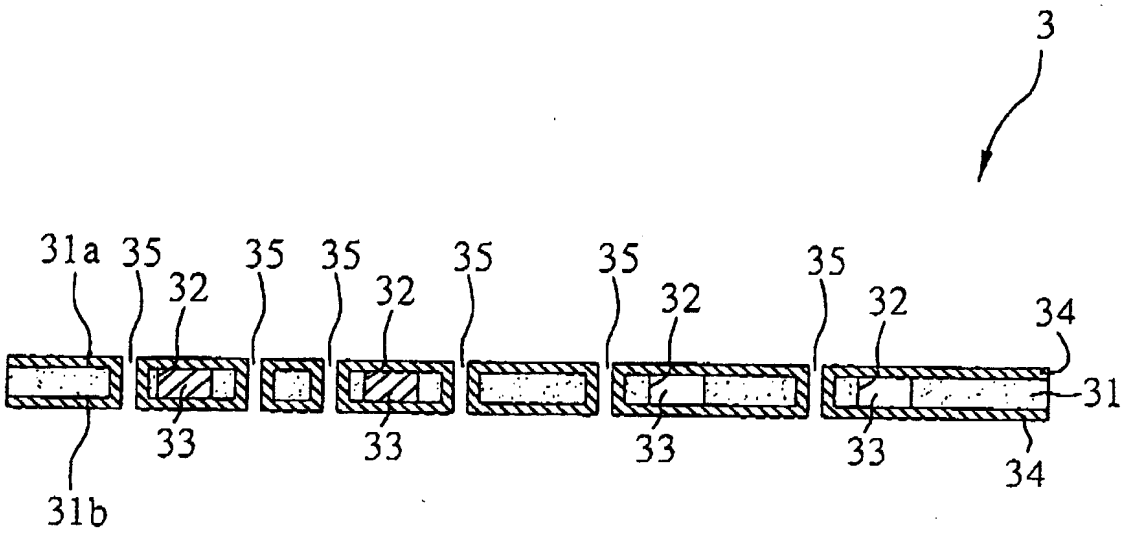

FIG. 3B